Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 8086/8088 signals
- List of other accessible microprocessor signals and extra acquisition channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for an 8086/8088 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

If you are using the optional DIP clip, the circuit board contains a 3 Amp fuse in series with the 5 Volt power plane. The fuse can be replaced with a discrete part if it opens. The 3 Amp fuse does not protect the circuitry when the power is supplied from a source other then the DIP clip.

The probe adapter accommodates the Intel 8086/8088 microprocessor in a 40-pin DIP package.

Configuration

The probe adapter does not require any configuration.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements
SUT DC Power Requirements	
Voltage	4.75-5.25 VDC
Current	I max (calculated) 200 mA I typ (measured) 130 mA
SUT Clock	
Clock Rate	Min. DC Max. 16 MHz
Minimum Setup Time Required	
Address, Data, Control	5 ns
Relative to CLK rising edge:	
S0~-S2~ inactive to active (MAX Mode only)	3.6 ns
RQ~/GTx~ (MAX Mode only)	3.6 ns
ALE (MIN Mode only)	3.6 ns
Relative to CLK falling edge:	
S0~-S2~ active to inactive (MAX Mode only)	15 ns *
HLDA (MIN Mode only)	16.5 ns *
RD~, WR~, INTA~ (MIN Mode only)	16.5 ns *
All Other Signals	5 ns
Minimum Hold Time Required	
All Signals	0 ns

Table 3–1: Electrical specifications (cont.)

Characteristics	Requirements	
	Specification	
	AC Load	DC Load
Measured Typical SUT Signal Loading		
CLK, S0~-S2~, MIN/MAX~, HOLD, HLDA, RD~, ALE	17 pf + 1 podlet	1, 22V10C + 1 podlet
LOCK~, INTA~	17 pf + 1 podlet	same as above
RESET	17 pf + 1 podlet	same as above
Other Signals	6 pf + 1 podlet	1 podlet

* **10 ns worst case PAL propagation delay and 5 ns logic analyzer setup time. The 8086/8088 microprocessors must meet this specification with plenty of margin.**

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specification*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

* **Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed 8086/8088 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

There are no applicable directives that apply to this product.

Figure 3–1 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

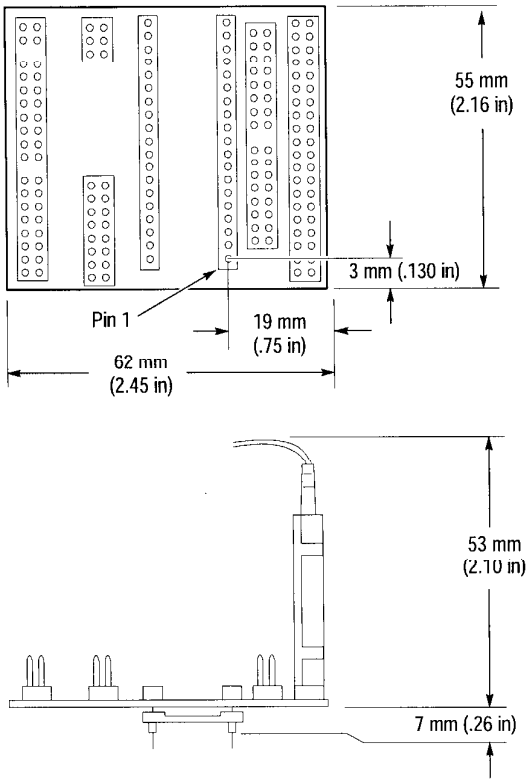

Figure 3–1: Dimensions of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–8 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the Most Significant Bit (MSB) descending to the Least Significant Bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal
- An equals sign (=) following a signal name indicates that it is double probed.

Table 3–4 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section: channel	8086/8088 signal name
19	A2:3	A19/S6
18	A2:2	A18/S5
17	A2:1	A17/S4
16	A2:0	A16/S3
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

Table 3–5 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default this channel group is displayed in hexadecimal.

Table 3–5: Data group channel assignments

Bit order	Section: channel	8086/8088 signal name
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

Table 3–6 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default this channel group is displayed symbolically.

Table 3–6: Control group channel assignments

Bit order	Channel	8086 MAX signal name	8086 MIN signal name	8088 MAX signal name	8088 MIN signal name
15	C2:7	RD~	RD~	RD~	RD~
14	A2:4	BHE~	BHE~	SS0	SS0~
13	C2:6	LOCK~	WR~	LOCK~	WR~
12	D2:4	S7	S7	S7	S7
11	D2:3	S6	S6	S6	S6
10	D2:2	S5	S5	S5	S5
9	D2:1	S4	S4	S4	S4
8	D2:0	S3	S3	S3	S3
7	C2:3	MN/MX~	MN/MX~	MN/MX~	MN/MX~
6	C2:5	QS1	INTA~	QS1	INTA~
5	C2:4	QS0	ALE	QS0	ALE
4	A2:7	S2~	M/IO~	S2~	IO/M~
3	A2:6	S1~	DT/R~	S1~	DT/R~
2	A2:5	S0~	DEN~	S0~	DEN~
1	C2:1	HLDA_D	HLDA_D	HLDA_D	HLDA_D
0	C2:0	RESET	RESET	RESET	RESET

Table 3–7 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–7: Misc group channel assignments

Bit Order	Channel	8086/8088 signal name: MAX mode	8086/8088 signal same: MIN mode
6	C3:6	CLK_B*	CLK B*
5	C3:5	TEST~*	TEST~*
4	C3:4	READY*	READY*
3	C3:3	INTR*	INTR*
2	C3:2	NMI*	NMI*
1	C3:1	RQ~/GT1~*	HOLDA
0	C3:0	RQ~/GT0~*	HOLD

* Signals not required for disasembly.

Table 3–8 shows the probe section and channel assignments for the clock probes (not part of any group) and the 8086/8088 signal to which each channel connects.

Table 3–8: Clock channel assignments

Channel	CLK or QUAL	8086/8088 signal name
CK:3	CLK	CLK
CK:2	QUAL	STATUS_D*
CK:1	QUAL	ALE_L
C2:3	QUAL	MIN/MAX~
C2:2	QUAL	EOC_D*
C2:1	QUAL	HLDA_D*
C2:0	QUAL	RESET

* Derived signals.

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–8, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires 8086/8088 signals using the TMS 101 software and probe adapter. This part of this chapter also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the 8086/88 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 8086/8088 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module Clocking State Machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figures 3–2 and 3–3 show sample points AC (Address sample point) and DC (Data sample point), in addition to MC (Master Clock sample point).

The TMS 101 uses a PAL (22V10C) on the probe adapter to decode the status lines and determine the sample points for the disassembler. The PAL decodes the 8086/8088 signals differently depending on the mode used (MAX or MIN):

- In MAX mode, the status lines become valid after the rising edge of CLK, and become invalid several cycles later after the falling edge of CLK to indicate the end of a bus cycle (see Figure 3–2). The PAL uses the S0~—S2~ lines to synthesize an output signal, STATUS, which allows the CSM to decode the cycles correctly. STATUS is only valid in MAX mode, and is sensed by the MIN/MAX~ line from the 8086/8088.

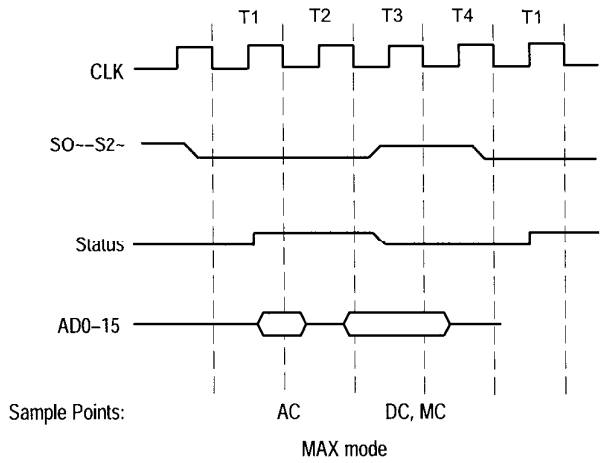

Figure 3–2: 8086/8088 Clocking in MAX Mode

- In MIN mode, the ALE line is latched on the rising edge of CLK. (See Figure 3–3.) This keeps it valid so the falling edge of CLK, which is used in the CSM, can read it and log in the address. This signal is ALE_L. A second signal, EOC_D, is generated by logically ORing the RD~, WR~, and INTA~ signals.

Figure 3–3 also shows when the various sample points are asserted. Sample points DC and MC occur at the end of a bus cycle, the only time the data is valid.

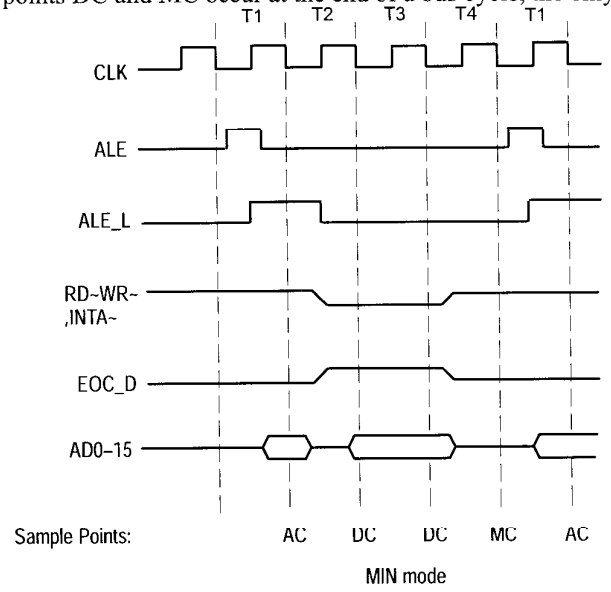

Figure 3–3: 8086/8088 Clocking in MIN Mode

Another signal generated by the PAL, HLDA_D, is also used differently depending on the mode. In MIN mode, HLDA passes straight through to the HLDA_D output. In MAX mode, HLDA is derived by tracking the pulses on the RQ~/GT0~ and RQ~/GT1~ lines.

DMA Cycles. DMA cycles may be observed only as seen by the 8086/8088 microprocessor. System buffering of the address, data, and control lines must be organized so they point to the 8086/8088, and enabled so the DMA cycles are visible to the probe adapter at the 8086/8088 socket. You may need to modify the SUT to meet these requirements if you want to monitor DMA cycles.

When DMA cycles are included, the HLDA signal is given special attention, and DMA cycles are distinguished from other ordinary 8086/8088 cycles. DMA cycles are included along with other 8086/8088-initiated cycles if the 8086/8088 bus transfer protocol is followed and if the SUT bus buffering topology provides adequate data visibility at the 8086/8088 socket. If these conditions are not met, a special sample is forced to record a transfer of bus mastership.

When DMA cycles are excluded, the CSM goes to an idle state whenever HLDA is asserted. The CSM does not log or store data while in this state, and remains in this state until HLDA is negated. Once HLDA is negated, the CSM resumes normal logging and data storage.

Clocking Options

The clocking algorithm for the 8086/8088 support has two variations: DMA Cycles Excluded and DMA Cycles Included.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–5. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

All 8086/8088 microprocessor signals are accessible on the probe adapter. In addition to the 8086/8088 socket, all 8086/8088 signals are also routed to a 40-pin square pin header (J900). This is provided so you can connect to soldered in 8086/8088 microprocessors (using optional cable) or to extra podlets. These signals can be useful for general purpose analysis. Remember that all signals are already assigned to channel groups and cannot be assigned to another channel group.

Table 3–9 shows the microprocessor signals available on J900 of the probe adapter.

Table 3–9: 8086/8088 signals on J900

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	GND	15	AD8	28	S1~_DIR~
2	+5V	16	MIN_MAX~	29	AD1
3	AD14	17	AD7	30	S0~_DIR~
4	AD15	18	RD~	31	AD0
5	AD13	19	AD6	32	QS0_ALE
6	A16_S3	20	RQ0_HOLD	33	NMI
7	AD12	21	AD5	34	QS1_INTA~
8	A17_S4	22	RQ1_HLDA	35	INTR

Table 3–9: 8086/8088 signals on J900 (cont.)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
9	AD11	23	AD4	36	TEST~
10	A18_S5	24	LOCK~_WR~	37	CLK
11	AD10	25	AD3	38	READY
12	A19_S6	26	RS _MIO~	39	GND
13	AD9	27	AD2	40	RESET
14	BHE~_S7				

Extra Channels

Table 3–10 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–10: Extra module sections and channels

Module	Section: channels
102-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0, Qual:1, Qual:0
136-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0, E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0
96-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.